Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

initiating a direct memory access; and

successively transferring data from a plurality of linked buffers in a first processor system to a plurality of linked buffers in a second processor system, wherein the successive transferring is via a first-in-first-out buffer in the first processor system to a first-in-first-out buffer in the second processor system.

Claim 2 (previously presented): The method of claim 1 wherein successively transferring data from the plurality of linked buffers includes successively transferring data from buffers arranged in a linked list on the first processor system to the plurality of linked buffers arranged in a linked list on the second processor system.

Claim 3 (previously presented): The method of claim 2 including providing the linked list with descriptors that indicate the status of each of said buffers.

Claim 4 (currently amended): The method of claim 3 including providing in the descriptors of the linked list flags that indicate whether a corresponding buffer is empty or full.

Claim 5 (previously presented): The method of claim 1 including transferring data between the plurality of linked buffers within a cellular telephone.

Claim 6 (previously presented): The method of claim 5 including transferring data between the first processor system that includes a baseband processor and the second processor system that includes a multimedia processor of the cellular telephone.

Claim 7 (canceled)

Claim 8 (canceled)

Claim 9 (currently amended): ~~The method of claim 1 including~~ A method comprising:

initiating a direct memory access;

successively transferring data from a plurality of linked buffers in a first processor system to a plurality of linked buffers in a second processor system; and

generating an interrupt when one of the linked buffers is empty, based on a flag associated with a descriptor for the one of the linked buffers, intercepting the interrupt, and automatically filling the one of the linked buffers.

Claim 10 (currently amended): The method of claim [[1]] 9 including determining whether one of the linked buffers that is to receive data is full based on a flag associated with a descriptor for the one of the linked buffers and if the one of the linked buffers is full, automatically generating an interrupt, intercepting the interrupt, and automatically emptying the one of the linked buffers.

Claim 11 (currently amended): An article comprising a computer-readable medium to store instructions that when executed enable a processor-based system to:

initiate a direct memory access; ~~and~~

successively transfer data from a plurality of linked buffers in a first processor system to a plurality of linked buffers in a second processor system; and

determine whether one of the linked buffers that is to receive data is full based on a flag associated with a descriptor for the one of the linked buffers and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

Claim 12 (previously presented): The article of claim 11 further storing instructions that enable the processor-based system to successively transfer data from the plurality of linked buffers arranged in a linked list on the first processor system to the plurality of linked buffers arranged in a linked list on the second processor system.

Claim 13 (previously presented): The article of claim 12 further storing instructions that enable the processor-based system to provide the linked list with descriptors that indicate the status of each of said buffers.

Claim 14 (currently amended): The article of claim 13 further storing instructions that enable the processor-based system to provide in the descriptors of the linked list flags that indicate whether a corresponding buffer is empty or full.

Claim 15 (previously presented): The article of claim 11 further storing instructions that enable the processor-based system to transfer data between the plurality of linked buffers within a cellular telephone.

Claim 16 (previously presented): The article of claim 15 further storing instructions that enable the processor-based system to transfer data between the first processor system that includes a baseband processor and the second processor system that includes a multimedia processor of the cellular telephone.

Claim 17 (canceled)

Claim 18 (canceled)

Claim 19 (previously presented): The article of claim 11 further storing instructions that enable the processor-based system to generate an interrupt when one of the linked buffers is empty, based on a flag associated with a descriptor for the one of the linked buffers, intercept the interrupt, and automatically fill the buffer.

Claim 20 (cancel)

Claim 21 (currently amended): A system comprising:

a processor; and

a storage coupled to said processor to store instructions that enable the processor to:

initiate a direct memory access; ~~and~~

successively transfer data from a plurality of linked buffers in a first processor system to a plurality of linked buffers in a second processor system; and

generate an interrupt when one of the linked buffers is empty, based on a flag associated with a descriptor for the one of the linked buffers, intercept the interrupt, and automatically fill the buffer.

Claim 22 (previously presented): The system of claim 21 wherein said storage stores instructions that enable the processor to successively transfer data from the plurality of linked buffers arranged in a linked list on the first processor system to the plurality of buffers arranged in a linked list on the second processor system.

Claim 23 (previously presented): The system of claim 22 wherein said storage stores instructions that enable the processor to provide the linked list with descriptors that indicate the status of each of said buffers.

Claim 24 (currently amended): The system of claim 23 wherein said storage stores instructions that enable the processor to provide in the descriptors of the linked list flags that indicate whether a corresponding buffer is empty or full.

Claim 25 (previously presented): The system of claim 21 wherein said plurality of linked buffers are within a cellular telephone.

Claim 26 (currently amended): The system of claim 25 wherein said processor [[is]] comprises a baseband processor, said system further including a multimedia processor.

Claim 27 (canceled)

Claim 28 (canceled)

Claim 29 (cancel)

Claim 30 (previously presented): The system of claim 21 wherein said storage stores instructions that enable the processor to determine whether one of the linked buffers that is to receive data is full based on a flag associated with a descriptor for the one of the linked buffers and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

Claim 31 (cancel)

Claim 32 (currently amended): The method of claim [[1]] 9, further comprising successively transferring the data directly from the first processor system to the second processor system via an internal bus of a wireless communication system.

Claim 33 (previously presented): The article of claim 11, further storing instructions that enable the system to successively transfer the data via a first-in-first-out buffer in the first processor system directly to a first-in-first-out buffer in the second processor system.

Claim 34 (previously presented): The article of claim 11, further storing instructions that enable the system to successively transfer the data directly from the first processor system to the second processor system via an internal bus of a wireless communication system.

Claim 35 (previously presented): The system of claim 21 wherein the first processor system comprises a first-in-first-out buffer coupled to the linked buffers.

Claim 36 (previously presented): The system of claim 21, wherein the system comprises a wireless communication system comprising the first processor system and the second processor system, the wireless communication system further comprising an internal bus to couple the first processor system and the second processor system.